M.Tech (ECE) 2nd Semester Examination
ELECTRONICS SYSTEM DESIGN
Subject Code: ECL 502

Time Allowed: 03 hours. Maximum Marks: 100

Before answering the question paper the candidate should ensure that they have been supplied the correct question paper. Complaints in this regard, if any, shall not be entertained after the examination.

Note: Attempt any five questions and all questions carry equal marks.

Section – A

1. (a) Design a binary toggle circuit that changes state with each rising edge of the clock input.
(b) Design a decoder of 4 to 16 with high Asserted output
   a) \( F_1(X,Y,Z,W) = \Sigma(2,6,9,11,13) \)
   b) \( F_2(X,Y,Z,W) = \Sigma(1,4,8,10) \)

2. Write short notes on the following:
   a) Clock skew
   b) Bus system for Tri-State.
   c) Clocking Aspects.
   d) Collector in wired logic

3. Using the method outlined, carryout the following conversion
   i. Convert S-R to J-K flip flop
   ii. Convert J-K to D flip flop

Section – B

4. Implement and design Bare-bones block diagram, detailed flow diagram, and MDS diagram for the SYSTEM CONTROLLER.

5. Write short notes on the following:
   a) Synchronous Counter
   b) Hazard
   c) Race
   d) PROM

6. Analyze the state diagram of its sequential behavior
   \( D_A = \overline{A}C + \overline{B}X \)
   \( D_B = \overline{B}A + BC \)
   Load = ABCX